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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,600	07/30/2001	Ping-Sheng Tseng	C5048AP07	8219

54698 7590 04/23/2009

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EXAMINER	
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ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
04/23/2009	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PING-SHENG TSENG, YOGESH GOEL, SU-JEN HWANG, JAMES LEE, and KUN-HSU SHEN

Appeal 2008-4146
Application 09/918,600
Technology Center 2100

Decided:[1] April 23, 2009

Before JAY P. LUCAS, ST. JOHN COURTENAY III, and THU A. DANG, *Administrative Patent Judges.*

DANG, *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

I. STATEMENT OF CASE

Appellants appeal the Examiner's final rejection of claims 1-37 under 35 U.S.C. § 134 (2002). We have jurisdiction under 35 U.S.C. § 6(b)(2002).

We AFFIRM.

A. INVENTION

According to Appellants, the invention relates to electronic design automation (EDA), and more particularly, relates to dynamically changing the evaluation period to accelerate design debug sessions (Spec. 3, ll. 3-5).

B. ILLUSTRATIVE CLAIM

Claim 1 is exemplary and is reproduced below:

1. A behavior processor system for operating a portion of a user design and interfacing with a host testbench process, comprising:

a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function; and

a testbench call back process for responding to the behavior level function in the reprogrammable logic element by sending signal to the host testbench process.

C. REJECTIONS

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Bunza	US 5,838,948	Nov. 17, 1998

IEEE Standard Hardware Description Language Based on the Verilog Hardware Description Language, IEEE Std 1364-1995 (1996) (hereinafter "IEEE Std").

Eduardo Do Valle Simoes, et al., *A 145MHz User-Programmable Gates Array*, Proc. Sixth IEEE International Workshop on Rapid System Prototyping, 226-232 (1995) (hereinafter "Simoes").

Claims 29 and 34 stand rejected under 35 U.S.C. § 112, second paragraph as containing unclear language[2];

Claims 1-3, 5-11, 13-15, 17-30, 32-34, and 36 stand rejected under 35 U.S.C. § 102(e) as anticipated by the teachings of Bunza;

Claims 4, 16, 31, and 35 stand rejected under 35 U.S.C. § 103(a) over the teachings of Bunza in view of IEEE Std; and

Claims 12 and 37 stand rejected under 35 U.S.C. § 103(a) over the teachings of Bunza in view of Simoes.

II. ISSUE

The issue is whether Appellants have shown that the Examiner erred in determining that:

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[2] Despite the Examiner's indication that the claims are "objected to under 35 USC 112 ¶ 2nd," (Ans. 15), we deem that the Examiner has intended that the claims be *rejected* under 35 U.S.C. § 112, second paragraph. For the sake of judicial economy, we will address this rejection under 35 U.S.C. § 112, second paragraph on this Appeal, and will not refer this matter to the Office of Petitions.

1) claims 29 and 34 contain limitations expressed in indefinite language under 35 U.S.C. § 112, second paragraph; and

2) Bunza discloses "a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function" (claim 1).

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Bunza

1. Bunza discloses a system 200 for simulation of a target hardware, wherein part of the target hardware is modeled by the processor emulator 202 and part of the target hardware is modeled by a hardware simulator 206 (col. 10, ll. 20-22; Fig. 6).
2. Bunza discloses a well-known teaching of using a reconfigurable circuitry 96, such as a field programmable gate array (FPGA), to emulate target circuitry functions (col. 9, ll. 8-12), and that system 200 includes microprocessor 76 which uses components such as the FPGA to form a hardware circuit emulation (col. 10, ll. 10-13).
3. Bunza discloses that most hardware simulators allow multiple levels of modeling abstraction from a switch or transistor level model to a high level behavioral model (col. 5, ll. 62-67).

4. Bunza discloses that, to avoid the problems of precluding unsynthesizable behavioral or high-level design representations, typical of early stages of design (col. 9, ll. 49-52), Bunza's invention allows for the early simulation of the target hardware and permits the parallel development of the target hardware and the target program (col. 9, ll. 62-64).

IV. PRINCIPLES OF LAW

35 U.S.C. § 112, 2nd paragraph

"The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention" 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 102

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted). "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) "In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art." *Id.* (citations omitted).

The *claims* measure the invention. *See SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). "[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)).

Of course, anticipation "is not an 'ipsissimis verbis' test." *In re Bond*, 910 F.2d 831, 832-33 (Fed. Cir. 1990) (citing *Akzo N.V. v. United States Int'l Trade Comm'n*, 808 F.2d 1471, 1479 n.11 (Fed. Cir. 1986)). "An anticipatory reference . . . need not duplicate word for word what is in the claims." *Standard Havens Prods., Inc., v. Gencor Indus., Inc.,* 953 F.2d 1360, 1369 (Fed. Cir. 1991).

V. ANALYSIS

Claims 29 and 34

Appellants appeal the Examiner's rejection based on his finding that claims 29 and 34 contain "limitations expressed in unclear language" since the Examiner considers claims 28 and 29 to be synonymous, as well as claims 33 and 34 (App. Br. 6). Appellants contend that "the scope of claims 28 and 29 is significantly different" because "[c]laims 28 and 29 separately claim which component, 'workstation' generally or 'testbench process' specifically, will service the signal" (*id.*) and that "the specification clearly

differentiates between the workstation of claim 33 and the testbench process of claim 34" (*id.* at 7). Thus, we consider whether the term "testbench process," as recited in claims 29 and 34, is indefinite under under 35 U.S.C. § 112, second paragraph.

After reviewing Appellants' Specification in view of the claimed invention, we agree with the Appellants. As set forth in the Specification at page 190, lines 25-27, "test bench process 3101 in software provides test bench data via line 3104a for the hardware model in the emulator 3103 to process." This definition of "test bench" is separate and distinct from "workstation 3100" (Spec. 190, l. 24; Fig. 99). As such, we find that the term "testbench" in claims 29 and 34 does distinctly set forth the subject matter which the applicant regards as his invention, as required by 35 U.S.C. §112, second paragraph.

Therefore, Appellants have shown the Examiner erred in concluding that claims 29 and 34 are indefinite under under 35 U.S.C. § 112, second paragraph. Accordingly, we reverse the Examiner's rejection of claims 29 and 34 under 35 U.S.C. § 112, second paragraph.

Claims 1, 27-29, and 32-34

Regarding claim 1, Appellants argue that Bunza "lacks any disclosure of a behavior level function being modeled in a reprogrammable logic element" (App. Br. 10) because "the term 'hardware simulator" as used in [Bunza] refers to a software program" (Reply Br. 8) which differs from

"reprogrammable logic elements (hardware devices)" (*id.* at 9). However, the Examiner finds that Bunza "clearly teaches that various abstraction levels including the behavioral level model can be put on a programmable logic element (like FPGA)" (Ans. 16). Thus, the issue that we address on appeal is whether Bunza discloses "a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function" (claim 1).

We begin our analysis by giving the claims their broadest reasonable interpretation. *See In re Bigio*, 381 F.3d at 1324. Furthermore, our analysis will not read limitations into the claims from the specification. *See In re Van Geuns*, 988 F.2d at 1184. Claim 1 simply does not place any limitation on what "reprogrammable logic element" means, includes or represents, other than that the reprogrammable logic element is "for modeling a hardware model of the portion of the user design that includes a behavior level function" (claim 1). Therefore, we will not confine the meaning of "reprogrammable logic elements" to the "hardware devices" definition provided in Appellants' arguments (Reply Br. 9).

Furthermore, we find that Appellants' argument that Bunza "lacks any disclosure of a behavior level function being modeled in a reprogrammable logic element" is not commensurate with the language of claim 1. That is, claim 1 does not recite any limitation in which the behavioral level function is "being modeled in a reprogrammable logic element" as Appellants contend. Rather, claim 1 recites that the reprogrammable logic element is

"for modeling a hardware model of the portion of the user design that includes a behavior level function." We construe the "reprogrammable logic element" to be an element that models a hardware model of a user design, wherein the user design includes a behavior level function.

We agree with the Examiner's finding that Bunza discloses the claimed "reprogrammable logic element" as set forth beginning at page 6 of the Answer, and including the Examiner's corresponding responsive arguments beginning at page 16 of the Answer.

Bunza discloses a system for simulation of target hardware (FF 1), wherein most hardware simulators allow multiple levels of modeling abstraction which includes high level behavioral model (FF 3). To avoid the problems of precluding high-level design representations typical of early stages of design, Bunza's system allows for the early simulation of the target hardware (FF 4).

We find that an artisan would have understood the simulation of Bunza to be a model of a portion of a user design that includes a behavior level function. Further, the artisan would also have understood the system of Bunza to be an element for modeling a hardware model of the portion of the user design that includes a behavior level function. We thus agree with the Examiner that Bunza discloses "a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function" (claim 1).

Contrary to Appellants' contention that Bunza "teaches away from this particular embodiment of the invention stating '[u]se of unsynthesizable behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators'" (App. Br. 9) (alteration in original), Bunza does not teach away from such limitations. Rather, Bunza's system ***avoids*** such problems in the prior art in the early stages of design, and instead ***allows*** for the early simulation of the target hardware (FF 4).

As to Appellants' argument that Bunza's "hardware simulator" differs from Appellants' "reprogrammable logic element" (Reply Br. 8-9), even if claim 1 recites a hardware device, such term "reprogrammable logic element" does not preclude a system of Bunza which includes hardware and software for modeling a hardware model. In fact, Bunza's system includes use of components such as the FPGA, similar to that of Appellants' invention, to form a hardware circuit emulation (FF 2).

Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting independent claim 1 under 35 U.S.C. § 102(e). As to independent claims 27 and 32, Appellants do not provide separate arguments with respect to the rejection of claim 1. Thus, we conclude that the Appellants also have not shown that the Examiner erred in rejecting claims 27 and 32, and claims 28, 29, 33, and 34, respectively falling with claims 27 and 32, under 35 U.S.C. § 102(e).

Claims 2, 3, 5, 6, and 30

As to claims 2, 3, 5, 6, and 30, Appellants also argue that Bunza "is devoid of a behavioral level function that includes a condition" (App. Br. 10) and "devoid of any teaching the signal includes an interrupt from the testbench call back process" (*id*. at 11), by repeating the argument that Bunza's "hardware emulators" "do not model a hardware portion of a user design that includes a behavioral level function" (Reply. Br. 11). However, as discussed above, we find that Bunza discloses a system, including hardware and software, that models a hardware portion of a user design that includes behavioral level function (FF 1-4). That is, as discussed above, we will not read the claimed "reprogrammable logic element" as Bunza's "hardware emulators" as Appellants contend.

The Examiner finds that Bunza "teaches that the behavioral level function includes a condition" (Ans. 7), and "detection of condition (condition trigger) in hardware . . . to interrupt the host test bench process (running on hardware simulator)" (*id*. at 20). Appellants do not show, in the Appeal Brief or Reply Brief, any argument to dispute that the Examiner has correctly shown where all the claimed "condition" and "interrupt" appear in the prior art.

Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting claims 2, 3, 5, 6, and 30 under 35 U.S.C. § 102(e).

Claims 7-11, and 36

As to claims 7-11, and 36, Appellants merely add that Bunza is "devoid of any teaching" of the claimed language (App. Br. 11-13). However, the Examiner finds that Bunza discloses such teachings (Ans. 7-11, 21-24). Appellants provide no argument to dispute that the Examiner has correctly shown where all the claimed elements appear in the prior art.

Accordingly, we conclude that Appellants have not shown that the Examiner erred in rejecting claims 7-11, and 36 under 35 U.S.C. § 102(e).

Claims 13-15 and 17-26

As to claim 13, Appellants argue that "[t]here is simply no teaching of using a behavior processor to model behavior functions in hardware in the cited section" of Bunza (App. Br. 15). However, claim 13 simply does not place any limitation on what "behaviour processor" means, includes or represents, other than that the behavior processor is "for modeling a second hardware model of a selected portion of the user design" (claim 13). Contrary to Appellants' argument that "a 'behavior processor' is an FPGA device" (Reply Br. 12), claim 13 does not define "behavior processor" as an FPGA device, and thus, we will not read "behavior processor" as an FPGA device, as Appellants contend.

We find that Appellants' argument that Bunza does not teach "using a behavior processor to model behavior functions in hardware" is not commensurate with the language of claim 13, since claim 13 does not recite

any limitation in which " behavioral functions" are "being modeled in hardware" by the behavior processor, as Appellants contend. In fact, claim 13 is silent as to any "behavioral functions." We construe the "behavior processor" to be an element that models a hardware model of a portion of user design.

We also note that such label "behavior" does not change the functionality of or provide any additional function to the claimed processor, but rather, is merely a label set forth for the processor. Such labels do not distinguish the claimed invention from the prior art.

As discussed above, Bunza discloses a system, including hardware and software, that models a hardware portion of a user design (FF 1-4). We find that an artisan would have understood the simulation of Bunza to be a model of a portion of a user design, and would have understood the system of Bunza to be a processor for modeling a hardware model of the portion of the user design.

As to Appellants' argument that "a 'behavior processor' is an FPGA device" (Reply Br. 12), even if claim 13 recites an FPGA device, such term "processor" does not preclude a system of Bunza which includes use of components such as the FPGA, similar to that of Appellants' invention (FF 2).

Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting claim 13 and claims 14, 15, and 17-26 falling with claim 13, under 35 U.S.C. § 102(e).

Claims 4, 12, 16, 31, 35, and 37

As to claims 4, 12, 16, 31, 35, and 37, Appellants do not provide separate arguments from the rejection of claims 1, 13, 27, and 32, from which they respectively depend. As discussed above, we find no deficiency regarding Bunza in the rejections of independent claims 1, 13, 27, and 32. Since Appellants have not provide separate arguments, we conclude that the Appellants have not shown that the Examiner erred in rejecting claims 4, 16, 31, and 35 over the teachings of Bunza in view of IEEE Std under 35 U.S.C. § 103(a); and claims 12 and 37 over the teachings of Bunza in view of Simoes under 35 U.S.C. § 103(a).

VI. CONCLUSIONS

(1) Appellants have shown that the Examiner erred in concluding that claims 29 and 34 contain indefinite language under 35 U.S.C. § 112, second paragraph.

(2) Appellants have not shown that the Examiner erred in finding that claims 1-3, 5-11, 13-15, 17-30, 32-34, and 36 are anticipated by the teachings of Bunza.

(3) Appellants have not shown that the Examiner erred in finding that claims 4, 16, 31, and 35 are unpatentable over the teachings of Bunza in view of IEEE Std.

(4) Appellants have not shown that the Examiner erred in finding that claims 12 and 37 are unpatentable over the teachings of Bunza in view of Simoes.

(5) Claims 1-37 are not patentable over the prior art of record.

VII. DECISION

The Examiner's decision rejecting claims 1-3, 5-11, 13-15, 17-30, 32-34, and 36 under 35 U.S.C. § 102(e) and rejecting claims 4, 12, 16, 31, 35, and 37 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc

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